Detectors to complement the MBA Lattice

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A Detectors Strategy for the APS Upgrade

While much progress has been made in x-ray detectors over the past twenty years, it has long been recognized that detectors fail to match the capability of synchrotron x-ray sources. Less-than-ideal detectors limit the breadth of available scientific programs, make inefficient use of APS x-rays, complicate experimental procedures, and lengthen the beamtime required to complete measurements. The proposed APS-Upgrade based on a multi-bend achromat will only result in additional unrealized potential unless planning includes appropriate consideration for expected detector needs.

Synchrotron Characteristic	Common Detector Limitation
High energy storage ring	Lack of mature sensor technologies efficient at high energy
Beam intensity	Dynamic range, count rate limitations, etc.
Timing properties of APS beam	Frame rate limitations of area detectors

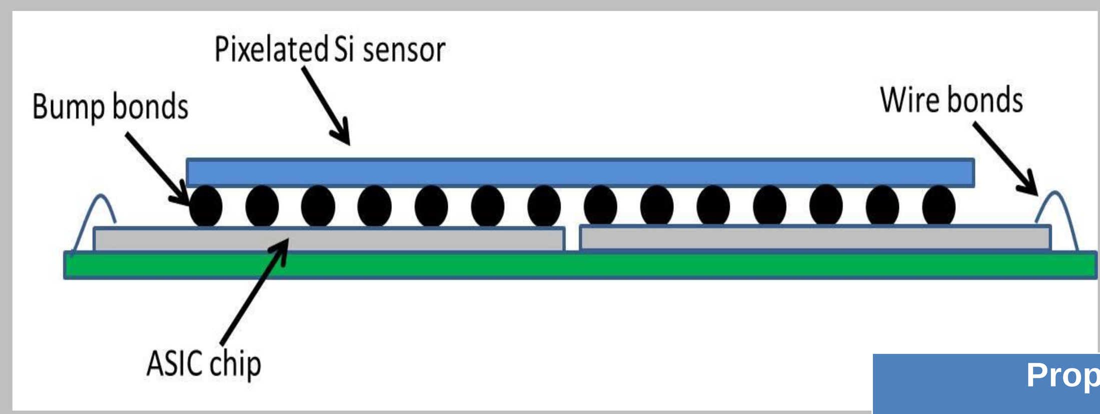
Spectroscopic Detectors	Area Detectors
High Resolution: Single eV resolution will open up new scientific opportunities	kHz and MHz frame rates for time-resolved reasearch
High Throughput : >10^5 cps per detector element	High flux detectors with modest pixel size
Greater sensor area, custom sensor geometries	High Energy Sensors

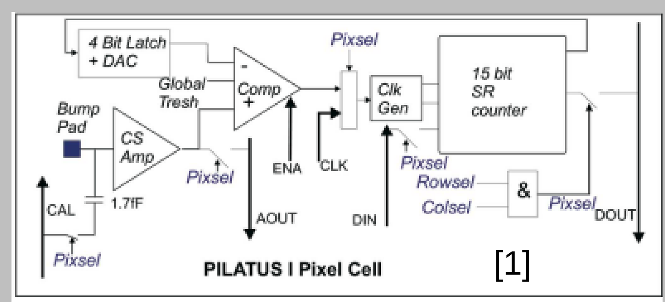
A review of detector needs prior to the MBA workshop revealed several key needs for spectroscopic and area detectors. Efficient strategies for satisfying these needs rely on both new commercial detectors and in-house development efforts. The best available commercial detectors will be purchase where appropriate. The APS-based effort in Microwave Kinetic Inductance Detectors (MKIDs) have the promise of single eV resolution and high count rates. To cover area detector needs un-met by commercial options, we are developing a new effort in pixelated area detectors.

Please See A. Miceli's poster for details of the MKIDs effort.

Hybrid Pixel Area Detectors

Flexibility for synchrotrons:
In traditional hybrid pixel detectors, an application specific integrated circuit (ASIC) is bump-bonded to a pixelated sensor. The sensor converts x-rays into an electronic signal and has commonly been made of silicon. The logic of the ASIC is also pixelated, and provides readout electronics to each channel of the sensor. The technology offers great flexibility as the ASIC logic can be tailored to create detectors for specific experimental techniques.





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Familiar technology:
Hybrid pixel detectors have been used at the APS since the first Pilatus detectors arrived in 2007. The pixel logic counts photons satisfying a lower level discriminator. Originally designed for protein crystallography, the Pilatus has found applications in many other x-ray techniques. A fast, reliable area detector with great signal-to-noise, the Pilatus has become an APS favorite.
2nd generation hybrid pixel detectors will soon be marketed by Dectris, the Medipix Collaboration, and ADSC. Most will be photon counting detectors capable of achieving frame rates of several kHz.

Room to Grow:
Despite achieving frame rates of several kHz, most commercially available 2nd generation hybrid pixel detectors will be similar to the original Pilatus – single photon counting detectors. Count rate limitations inherent in this technology may limit their suitability for an upgraded APS implementing an MBA lattice. Detectors based on integrating logic will record higher signal levels and facilitate novel experimental techniques.

Properties of Current Hybrid Pixel Detectors (Pilatus)

Detector Property	Pilatus Implementation	Comments
Sensor	350 mm – 1000 mm pixelated silicon	
Efficiency	Si: 56% efficient at 15 keV, but drops to 17% at 25 keV	Assumes 350 mm thick Si sensor. Never sold with Hi-Z sensor.
Pixel size	175 mm	Commonly interpreted as spatial resolution of detector.
Frame rate	300 Hz	Based on Pilatus 100K; rate slows for larger detectors.
Dynamic range	20 bits (~1M counts)	Single photon counting sensitivity with lower-level discriminator.

Two Area Detectors Optimized for APS-U:

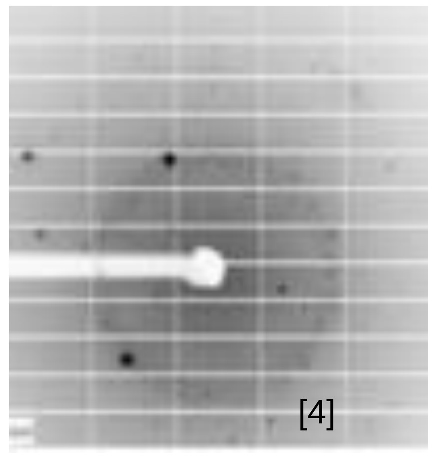
Plans are being developed for two fast area detectors to complement the APS Upgrade:

- The Fermi-Argonne Semiconductor Pixel Array X-ray detector (FASPAX) will use in-pixel analog storage to achieve a burst image rate of 13 MHz. FASPAX will record high resolution movies for time-resolved applications.
- CDI Detector: A high dynamic range area detector with fine pixels for coherence-based science.

The development is planned as a collaborative effort between the APS Detectors Group and the Fermilab ASIC Design Group.

Properties of Proposed Area Detectors

Detector Property	FASPAX	CDI Detector
Sensor	750 μm silicon 500 μm CdTe	
Dynamic Range	10^5 x-rays per pixel per x-ray pulse	
Readout logic	Integrating with in-pixel analog storage	Integrating with single frame storage for high duty factor.
Pixel size	100 μm	50-60 μm
Frame rate	13 MHz burst image rate (~3kHz average)	~few kHz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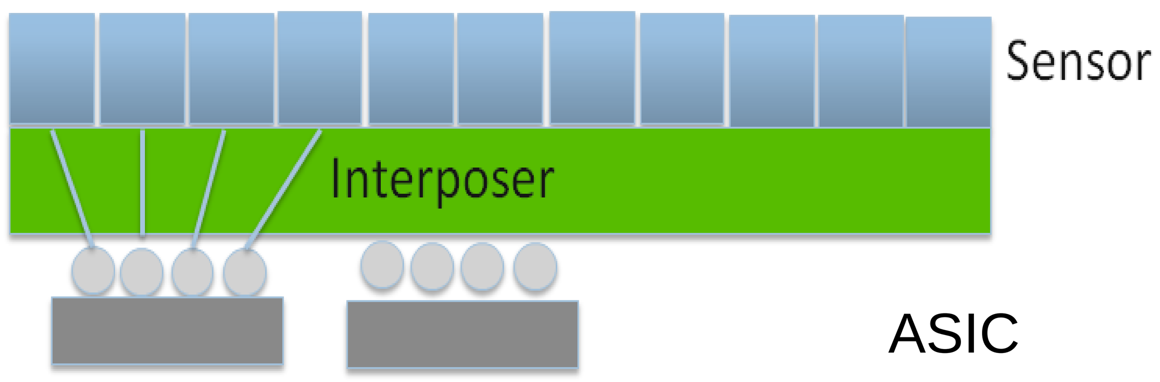
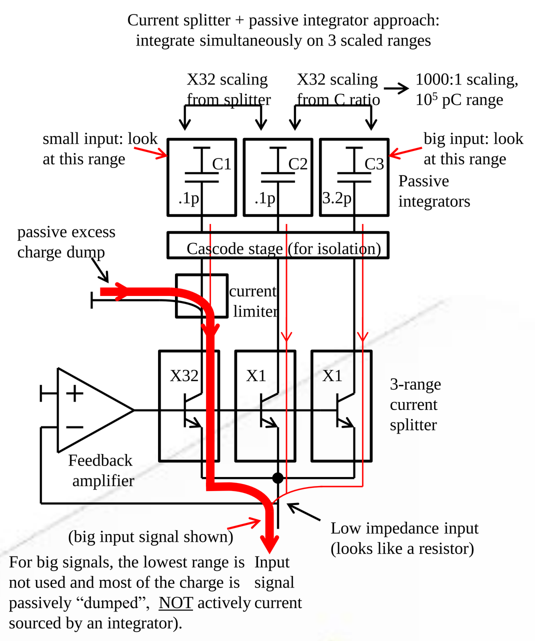
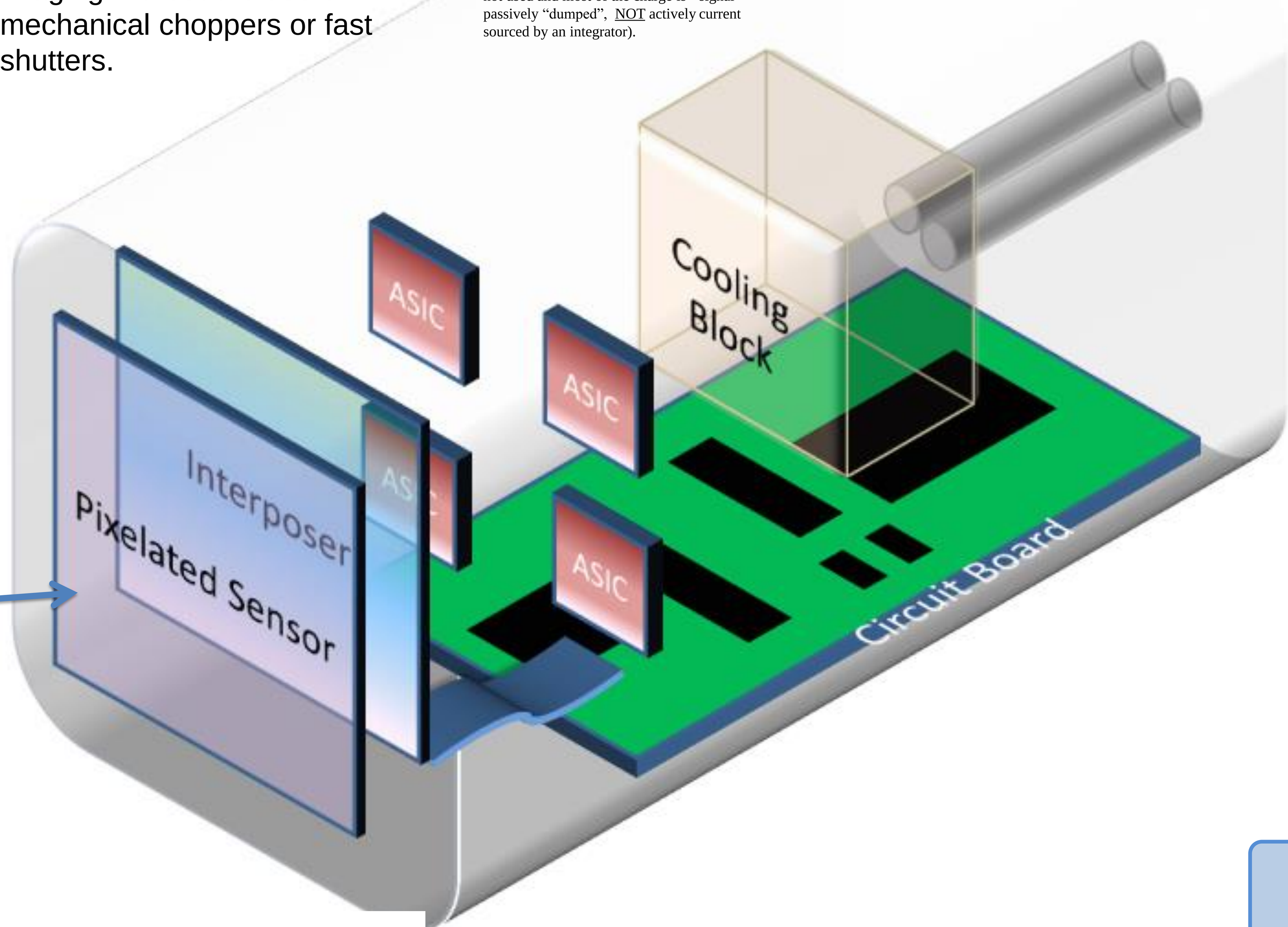
Unique sensor geometry:
Traditional hybrid pixel detectors are based on a modular construction where ~12 ASICs are directly bump-bonded to a modestly sized silicon sensor. Inactive regions on the edge of the module have typically been required for wire bonding to the ASIC, resulting in coverage gaps between modules.

We propose to investigate a gap-less sensor employing an interposer made from glass or silicon. Inserted between the sensor and ASICs, the interposer will eliminate the need for wire bonding. Traces on the interposer will provide power to the chips and read out data.

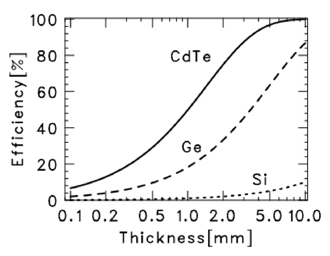


Integrating Circuit with 3-Stage Gain for High Dynamic Range:
A novel passive integrator based on current splitting will permit high dynamic range. Modest storage capacitor requirements will permit smaller pixel sizes. Self-selecting three stage gain will properly handle both single photon signals and 10^5 photons per pixel per x-ray pulse.
Implemented in FASPAX, this circuit will allow single-bunch imaging without the use of mechanical choppers or fast shutters.





Hi-Z Sensors:
Both detectors will accommodate standard silicon sensors as well as CdTe sensors available from Acrorad [5] for good detection efficiency at high energies. The proposed 500 μm-thick sensor is ~50% efficient at 100 keV.

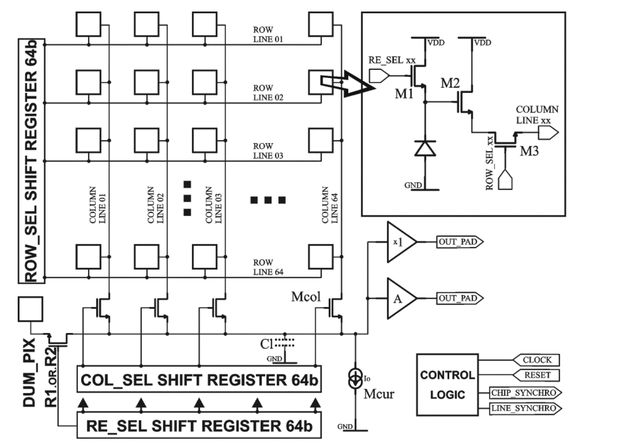


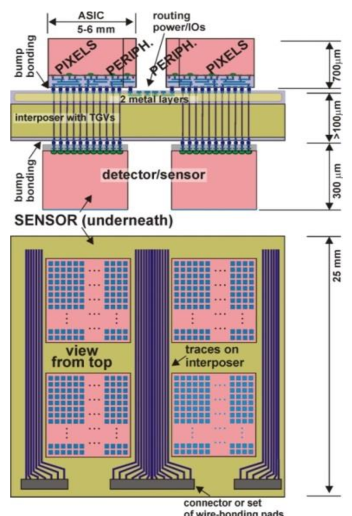
Sensor Efficiency vs. thickness at 100 keV.

Current Status and Plans:
Plans are currently being developed for an R&D effort through the APS Upgrade. A three year program, the R&D effort will focus on prototyping the sensor, ASIC, and interposer required for both detectors. Overall goals include:

- Production of two prototype ASICs for investigation and optimization of pixel logic.
- Investigation of prototype sensors in both silicon and CdTe.
- Production of a prototype interposer in glass or silicon
- Full x-ray testing of all prototypes to determine optimal designs.

Prototype ASICs:
5mm x 5mm ASICs will be produced using a multi-project wafer fabrication through MOSIS. The chips will implement a simplified readout and control structure.





Prototype Interposer:
A small 1" x 1" interposer will be designed and fabricated. Sensors will be bonded to the front, and prototype ASICs to the back. Performance of the interposer assembly will be compared to chips directly bump-bonded to a sensor to determine how the interposer affects detector performance.

Plans for the R&D program have been drafted and are currently being implemented into the APS-Upgrade's management software systems.

References

[1] Ch. Broennimann et al., *J. Synchrotron Rad,* 13 (2006), 120-130.
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[5] http://www.acrorad.co.jp/us/
[6] arXiv:astro-ph/0107398v1

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